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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/683,944	10/10/2003	Steven P. Young	X-1392-1P US	2771

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/683,944	YOUNG, STEVEN P.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-16,24-26,28,29 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-16,24-26,28,29 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 1-9 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on March 29, 2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10-16, 24-26, 28-29 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Langhammer et al. (US PAT No. 6,538,470).

Regarding claim 10, Fig. 9 of Langhammer et al. teaches an integrated circuit, comprising circuitry having programmable functions (LABs) and programmable interconnects (interconnect structure shown in Figs. 3 and 4), the IC further comprising: a plurality of homogeneous columns (LAB columns 108, I/O columns, 128) and wherein each of the homogeneous columns starts at one side of the IC and ends at an opposite side of the IC (LAB and I/O columns start at the top and end at the bottom of the floor plan), and wherein a first column of the plurality of homogeneous columns comprises a first set of substantially identical circuit elements of a first circuit type (LABs) substantially filling the first column, and a heterogeneous column (processing block 110

being a column comprises of INPUT REG, MULTIP, PIPELINE W/BYPASS, ADD/SUB/ACC, OUTPU SEL/REG) having configuration logic (register circuit 134 having programmable inversion capability, i.e. configurable logic) and a clock management circuit element (independent sets of clock being provided and clear signals 158 being provided for input register circuit, i.e. clocks signals are being routed or managed).

Regarding claim 11, Fig. 9 of Langhammer et al. teaches the integrated circuit of claim 10: wherein a second column (column 128 from left edge of the floor plan) of the plurality of homogeneous columns comprises a second set of substantially identical circuit elements of a second circuit type (column is filled with I/O circuit) substantially filling the second column, and wherein a third column (column 128 from right edge of the floor plan) of the plurality of homogeneous columns comprises a third set of substantially identical circuit (column is filled with I/O circuit) elements of a third circuit type substantially filling the third column (the third circuit type is the same as the second circuit type I/O).

Regarding claim 12, Fig. 9 of Langhammer et al. teaches the integrated circuit of claim 10 wherein the heterogeneous center column further comprises an input/output block (INPUT REG column and OUTPUT SEL/REG column).

Regarding claim 13, Fig. 9 of Langhammer et al. teaches the integrated circuit of claim 10 where the first circuit type is selected (LAB is selected for the first column from a group consisting of LAB, I/O, REG, MULTIP, ADD/SUB) from a group consisting of a Configurable Logic Block (LAB), a Multi-Giga Bit Transceiver (MGT) type, a Block Random Access Memory (Register being memory), a fixed logic type (MULTIP fixed for multiplication), an Input/Output Interconnect (PIPELINE W/BYPASS), and an Input/Output Block type (I/O).

Regarding claim 14, Fig. 9 of Langhammer et al. teaches the integrated circuit of claim 13 where the fixed logic type comprises a Digital Signal Processor (134 including scan chains used a logic in signal processing e.g. FIR filter; col. 20, lines 40-44), a multiplier circuit type (136), an arithmetic circuit type (144), an application specific circuit type (138 pipeline register circuits).

Regarding claim 15, Fig. 9 of Langhammer et al. teaches the integrated circuit of claim 10 where the integrated circuit further comprises a field programmable gate array (FPGA is a programmable logic device).

Regarding claim 16, Fig. 9 of Langhammer et al. teaches the integrated circuit of claim 10 where integrated circuit further comprises a programmable logic device (see ABSTRACT).

Regarding claim 24, Fig. 9 of Langhammer et al. teaches an integrated circuit comprising: a heterogeneous center column (processing block 110 being a center column comprises of INPUT REG, MULTIP, PIPELINE W/BYPASS, ADD/SUB/ACC, OUTPU SEL/REG) having configuration logic (register circuit 134 having programmable inversion capability, i.e. configurable logic) and a clock management circuit element (independent sets of clock being provided and clear signals 158 being provided for input register circuit, i.e. clocks signals are being routed or managed), a plurality of columns (see Fig. 9) and wherein each of the columns starts at one side of the IC and ends at an opposite side of the IC (top side to bottom side of Fig. 9), wherein a first column of the plurality of columns comprises a first set of substantially identical circuit elements of a first circuit type (LAB filled in the first column) substantially filling the first column, wherein a second column of the plurality of columns comprises a second set of substantially identical circuit elements of a second circuit type (I/O filled in the second column) substantially filling the second column.

Regarding claim 25, Fig. 9 of Langhammer et al. teaches the integrated circuit of claim 24 further comprising circuitry having programmable functions and programmable interconnects (LABs are programmable and the interconnection shown in Figs. 3 and 4).

Regarding claim 26, Fig. 9 of Langhammer et al. teaches the integrated circuit of claim 25 where the first, and second circuit types have a circuit type selected (the selected first, second and third types are LAB, I/O, and INPUT REG respectively) from a

group (group consisting of LAB, I/O, REG, MULTIP, ADD/SUB) consisting of a Configurable Logic Block (LAB) type, a Multi-Giga Bit Transceiver type, a Block Random Access Memory type, a Digital Signal Processor, an arithmetic circuit type , an Input/output Interconnect circuit type, an Input/output Block type, and an application specific circuit type.

Regarding claim 28, Fig. 9 of Langhammer et al. teaches the integrated circuit of claim 24 where the substantially identical circuit elements are substantially identical tiles (LABs are substantially identical tiles).

Regarding claim 29, Fig. 9 of Langhammer et al. teaches the integrated circuit of claim 28 wherein each tile comprises a functional element coupled to a switch matrix (Fig. 3 and 4 shows interconnect matrix).

Regarding claim 34, Fig. 9 of Langhammer et al. teaches an integrated circuit comprising circuitry having programmable functions (LABs) and programmable interconnects (interconnect structure shown in Figs. 3 and 4), the IC further comprising a heterogeneous center column (processing block 110 being a center column comprises of INPUT REG, MULTIP, PIPELINE W/BYPASS, ADD/SUB/ACC, OUTPU SEL/REG) having configuration logic (136, 138,144 are configurable logic performing a configured logic e.g. nxn bit multiplier) and a clock management circuit element (independent sets of clock being provided and clear signals 158 being provided for input

register circuit, i.e. clocks signals are being routed or managed), and an input/output block (input registers 134, Output Sel. Register 146); a plurality of homogeneous columns (108s, 128s) wherein each of the homogeneous columns starts at one side of the IC and ends at an opposite side of the IC (top side to bottom side of Fig. 9), and where

in a first column of the plurality of homogeneous columns comprises a first set of substantially identical circuit elements of a first circuit type (LAB filled in the first column) substantially filling the first column.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Cho
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Art Unit 2819